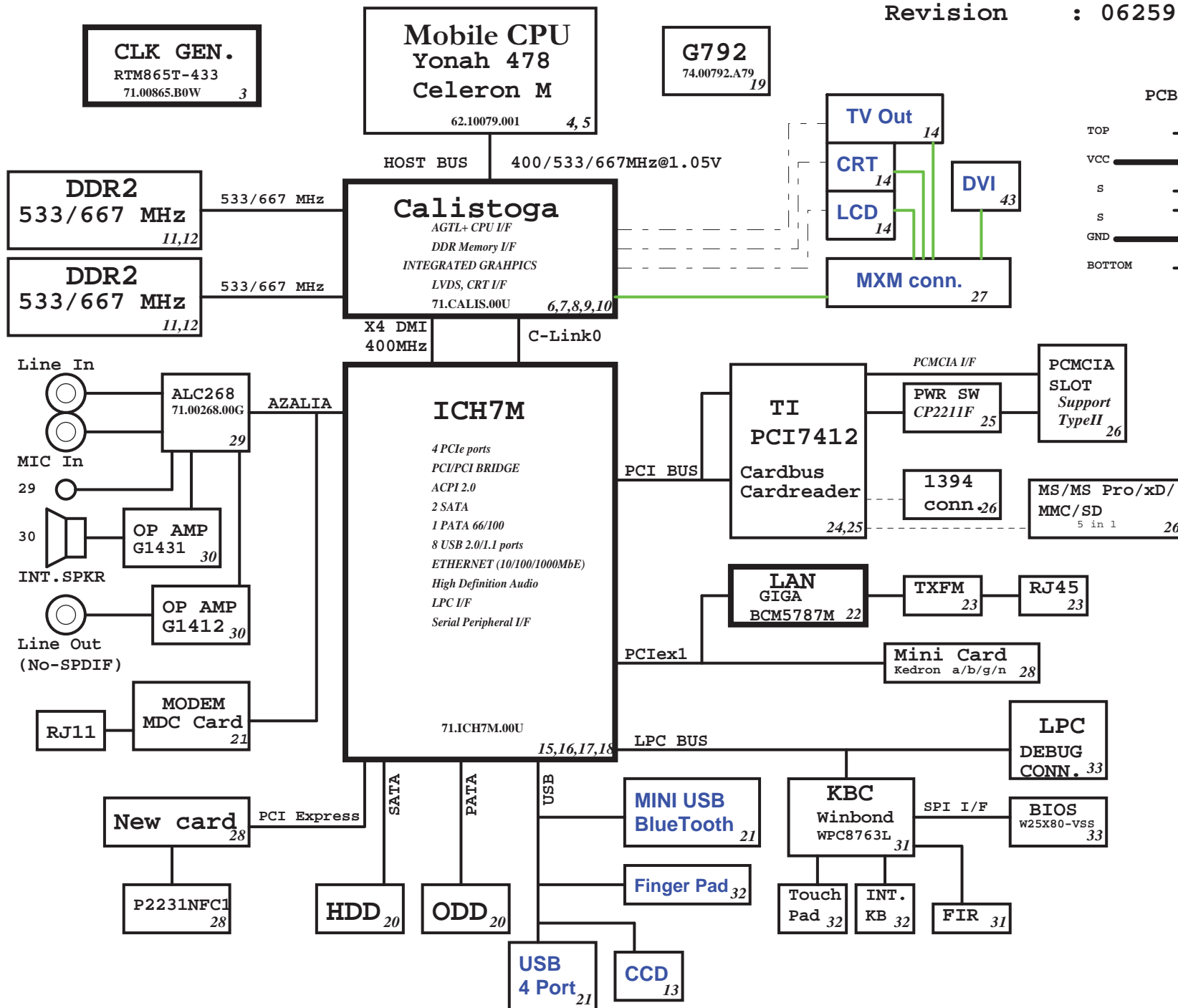


Dallen Block Diagram

Project code: 91.4V401.001
PCB P/N : 48.4T307.0SA
Revision : 06259 -1



SYSTEM DC/DC MAX8744 37	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 (6A) 5V_S5 (6A) 5V_AUX_S5
SYSTEM DC/DC Max8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (12A) 1D8V_S3 (8.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL531230 39	
3D3V_S0	2D5V_S0 (130 mA)
APL5912 39	
1D8V_S3	1D5V_S0 (5A)
ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPI17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSusl_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSusl_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance/ Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing

History

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

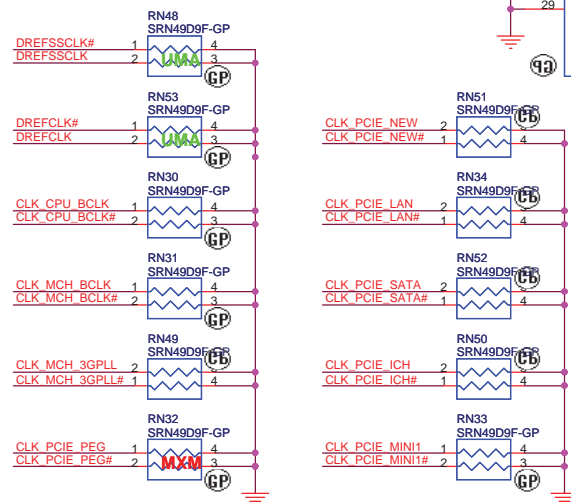
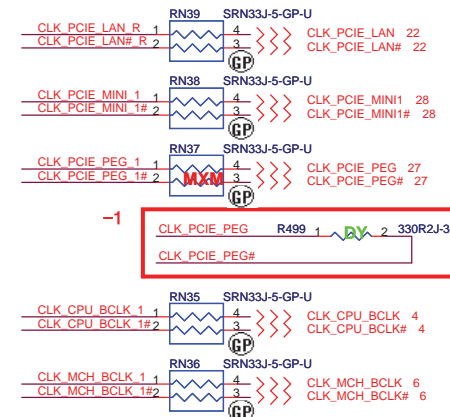
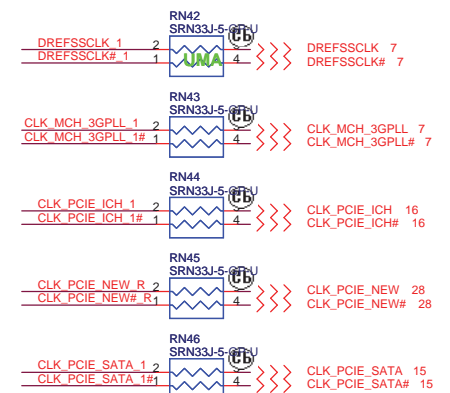
USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

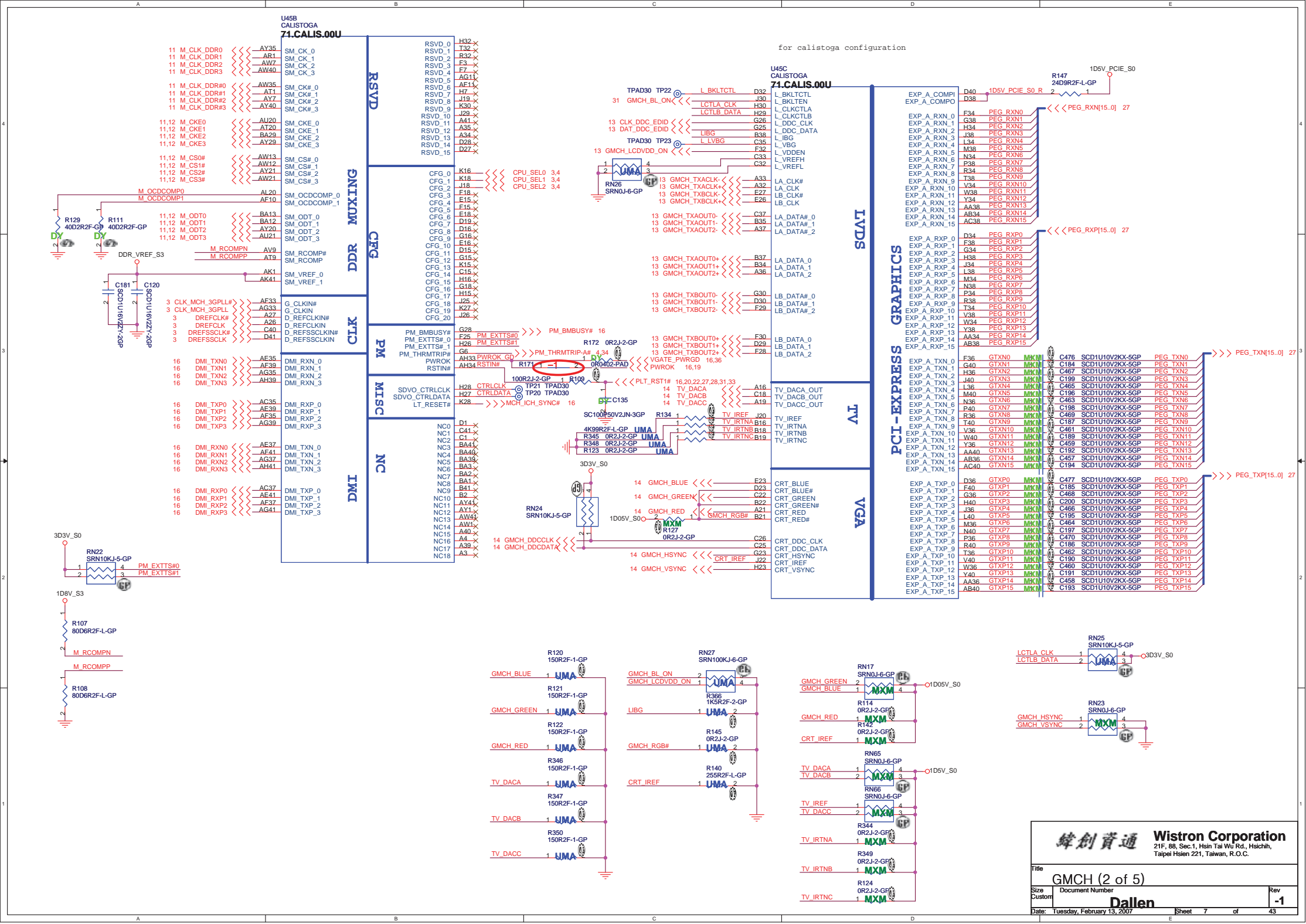
EDS 17050 0.71 page 7

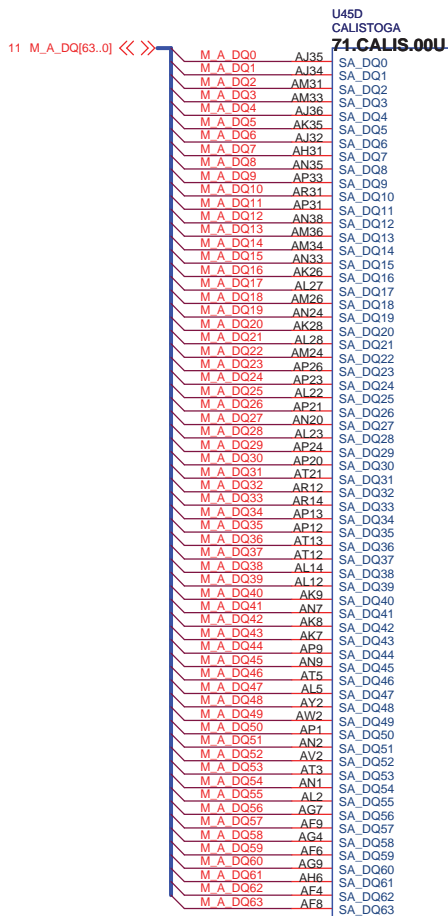
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWOR in signal.

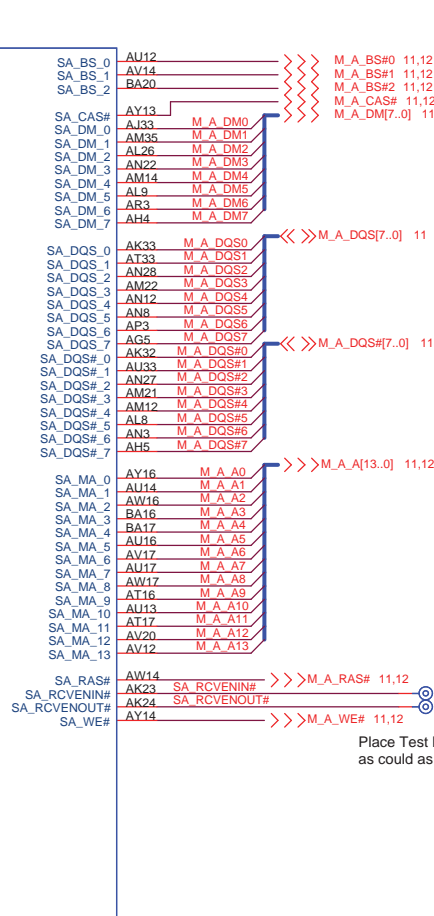


FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

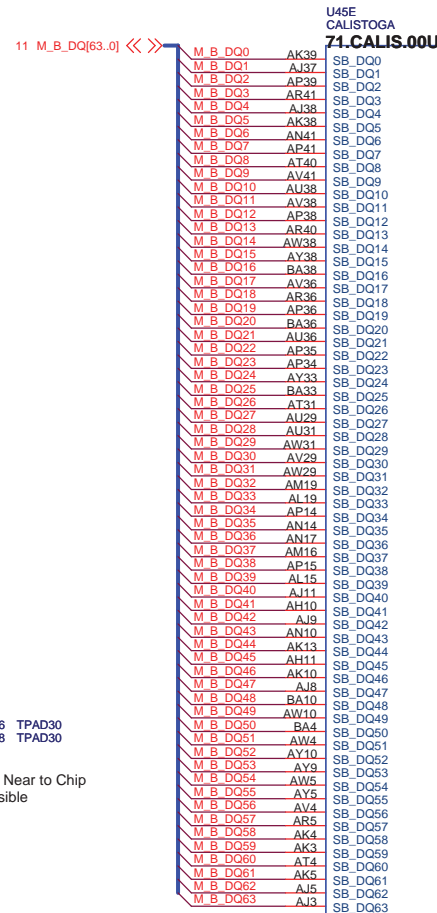




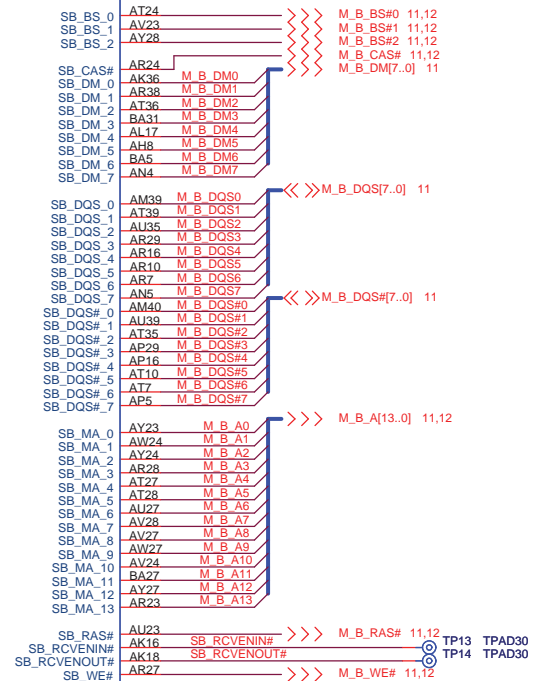
DDR SYSTEM MEMORY A



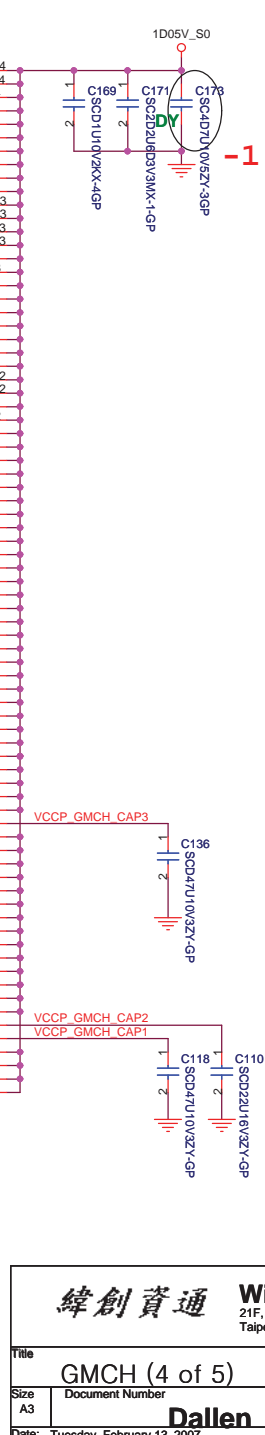
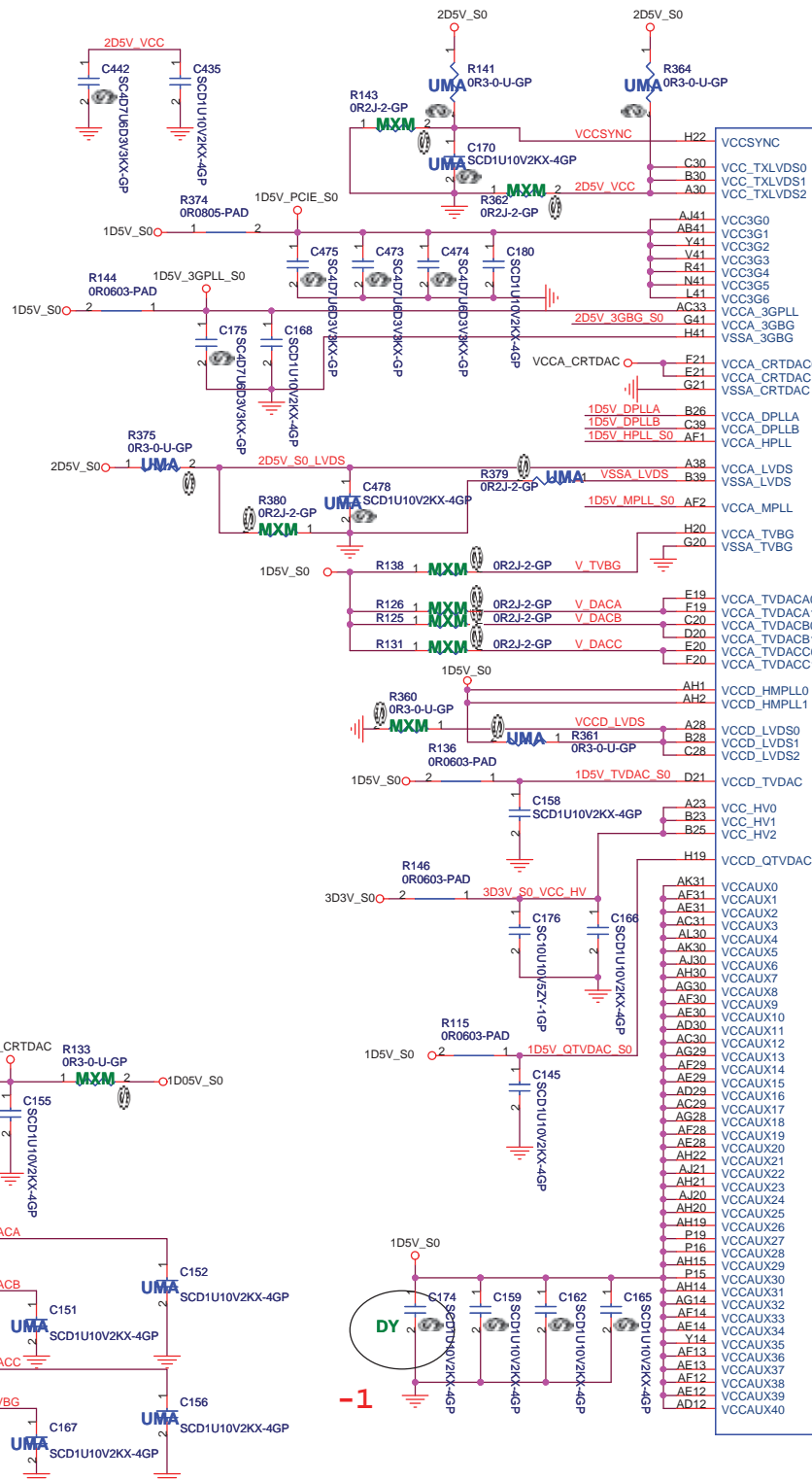
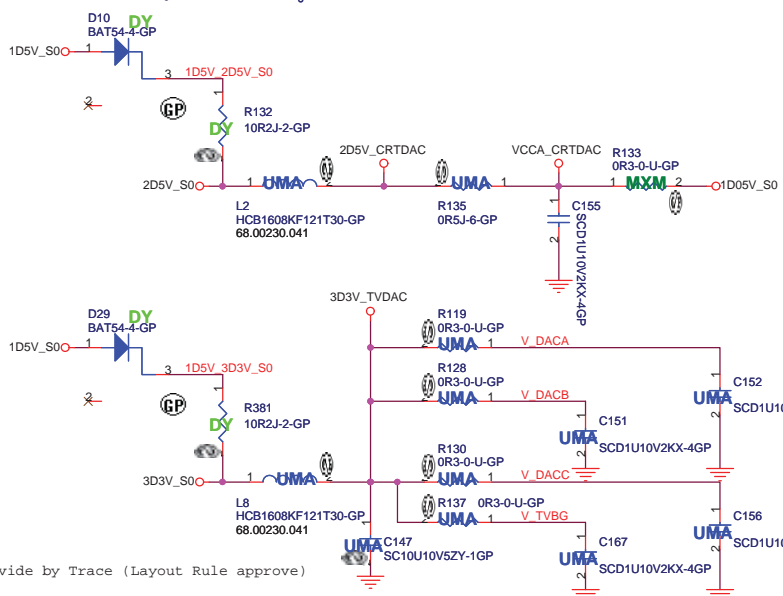
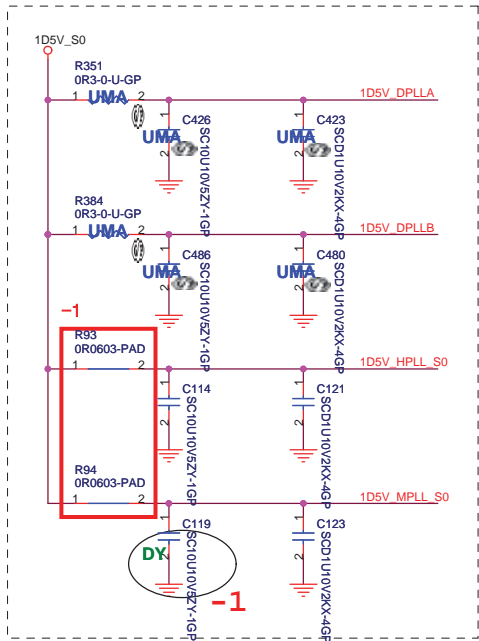
Place Test PAD Near to Chip
as could as possible



DDR SYSTEM MEMORY B



Place Test PAD Near to Chip
as could as possible



緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



DM2
DDR2-200P-22-GP-U1

High 9.2mm
62.10017.A61

DDR clock pairs SWAP

Place near DM2

M_CLK_DDR3

EC130
SC10P50V2JN-4GP

M_CLK_DDR#3

M_CLK_DDR2

EC17
SC10P50V2JN-4GP

M_CLK_DDR#2

DM1 SKT-SODIMM2002U3GP
High 5.2mm
62.10017.661

Place near DM1

M_CLK_DDR0

EC128
SC10P50V2JN-4GP

M_CLK_DDR#0

M_CLK_DDR1

EC16
SC10P50V2JN-4GP

M_CLK_DDR#1

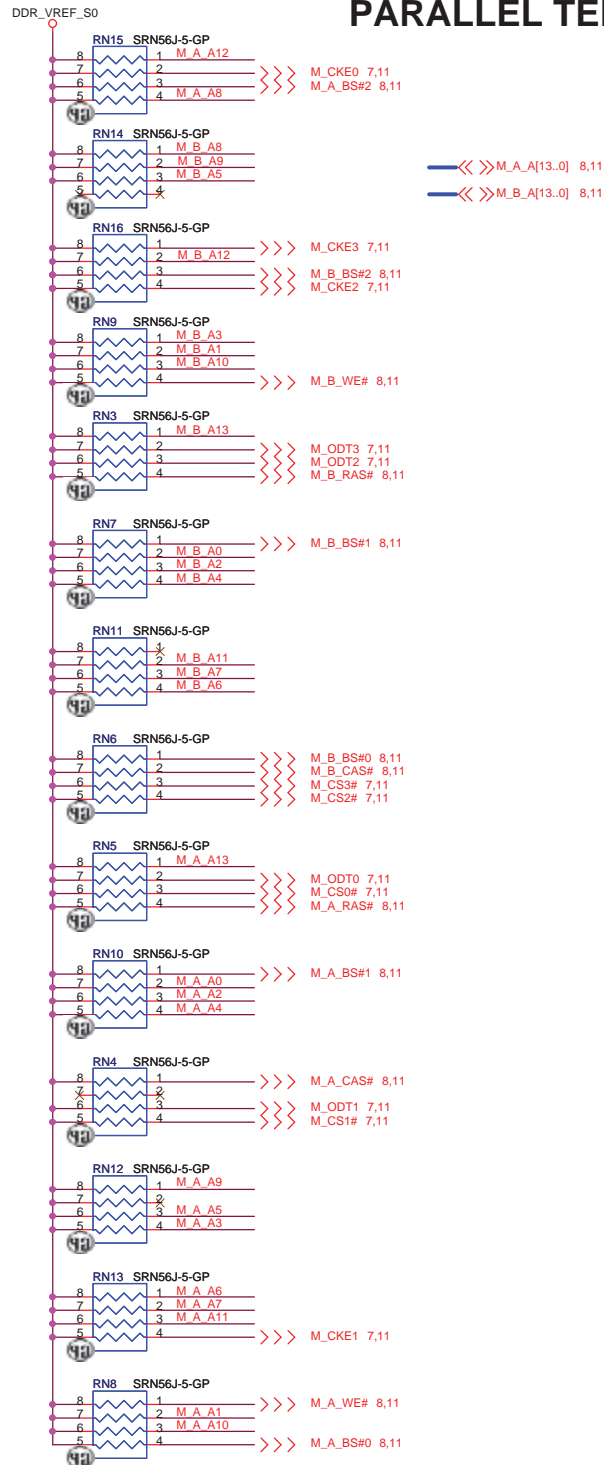
NORMAL TYPE

NORMAL TYPE

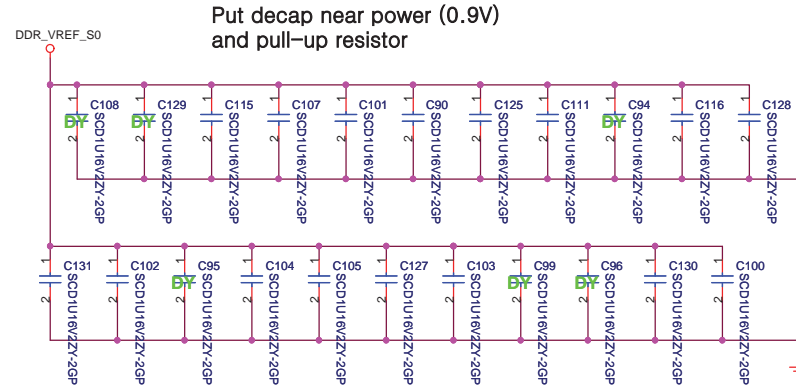
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Socket
Size: Document Number
Custom: Dallen
Date: Tuesday, February 13, 2007
Sheet: 11 of 43

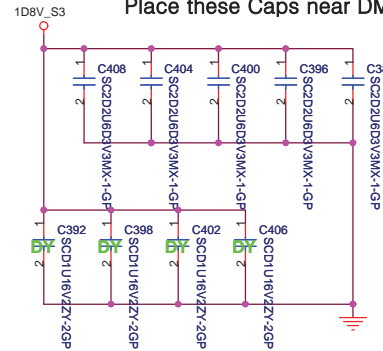
PARALLEL TERMINATION



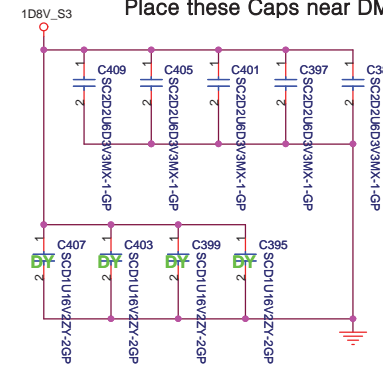
Decoupling Capacitor



Place these Caps near DM1



Place these Caps near DM2



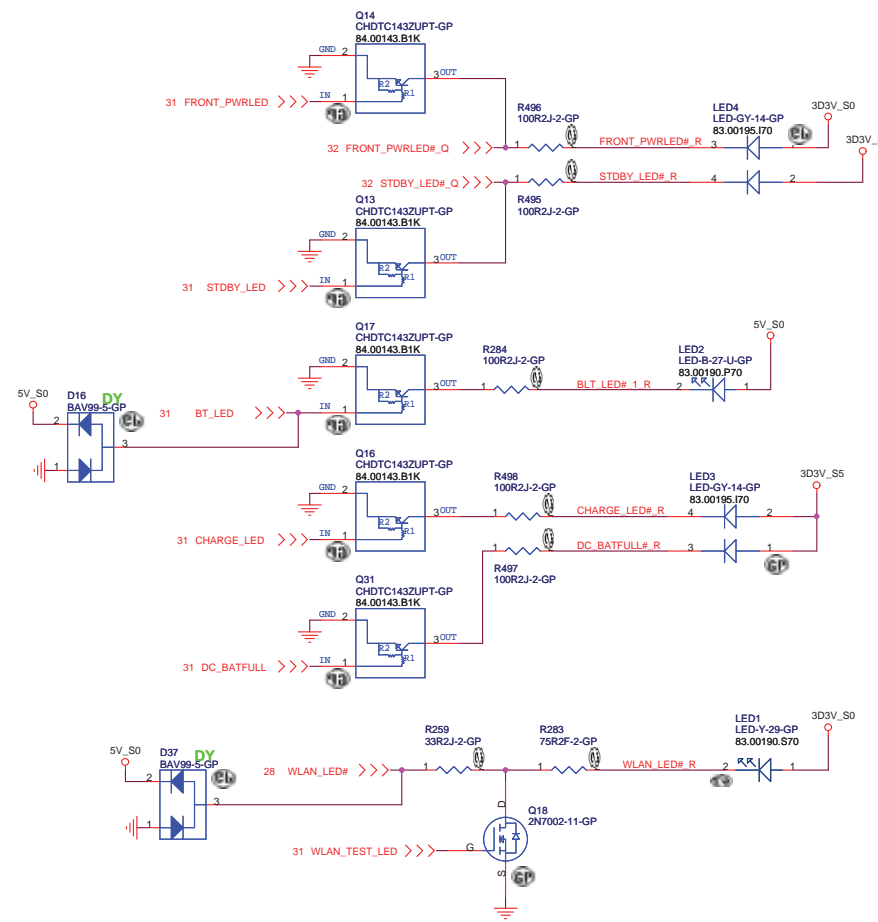
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		DDR2 Termination Resistor	
Size	Document Number	Rev	
A3		-1	
Date:	Tuesday, February 13, 2007	Sheet	12 of 43

Dallen

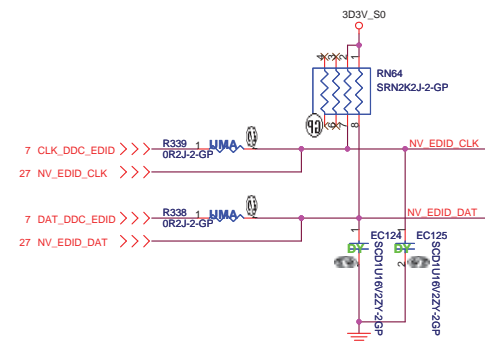
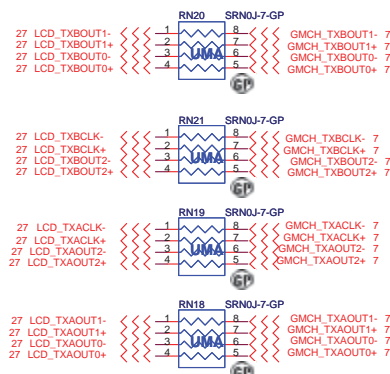
Sheet 12 of 43

Rev -1



```

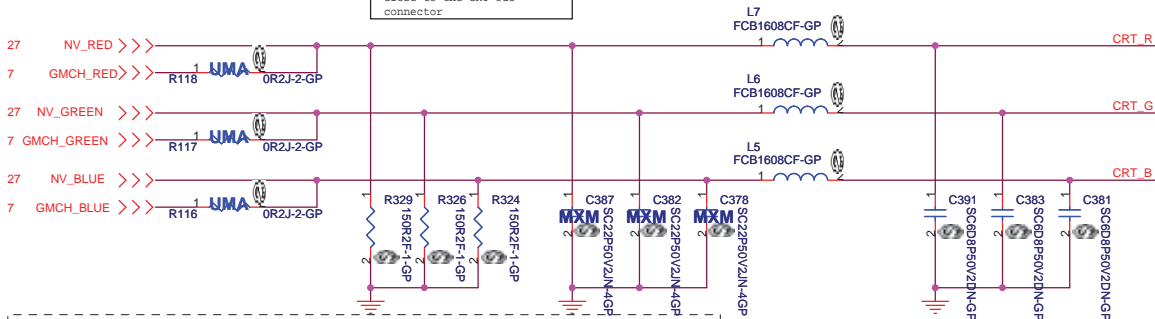
graph TD
    LCD_conn[LCD conn.] --- 8P4Rs[8P4Rs]
    LCD_conn --- MXM[MXM]
    8P4Rs --- UMA_NB[UMA (NB)]
    MXM --- MXM_label[MXM]
  
```



CRT I/F & connector

Layout Note:
Place these resistors
close to the CRT-out
connector

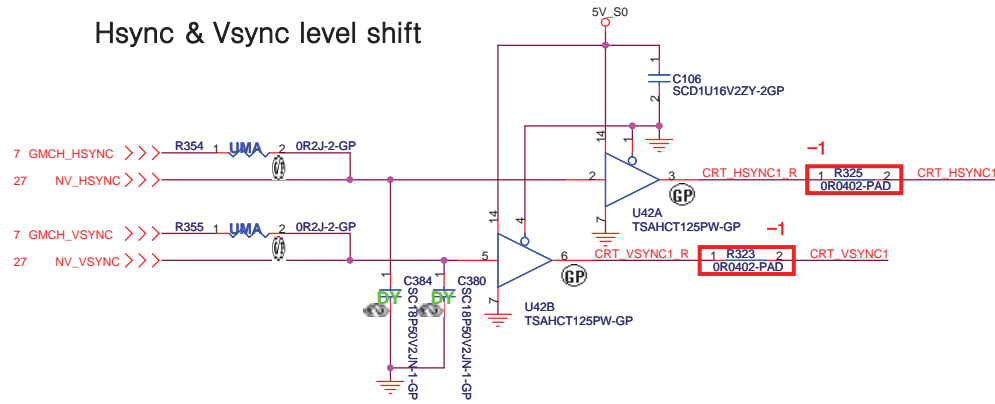
Ferrite bead impedance: 10 ohm@100MHz



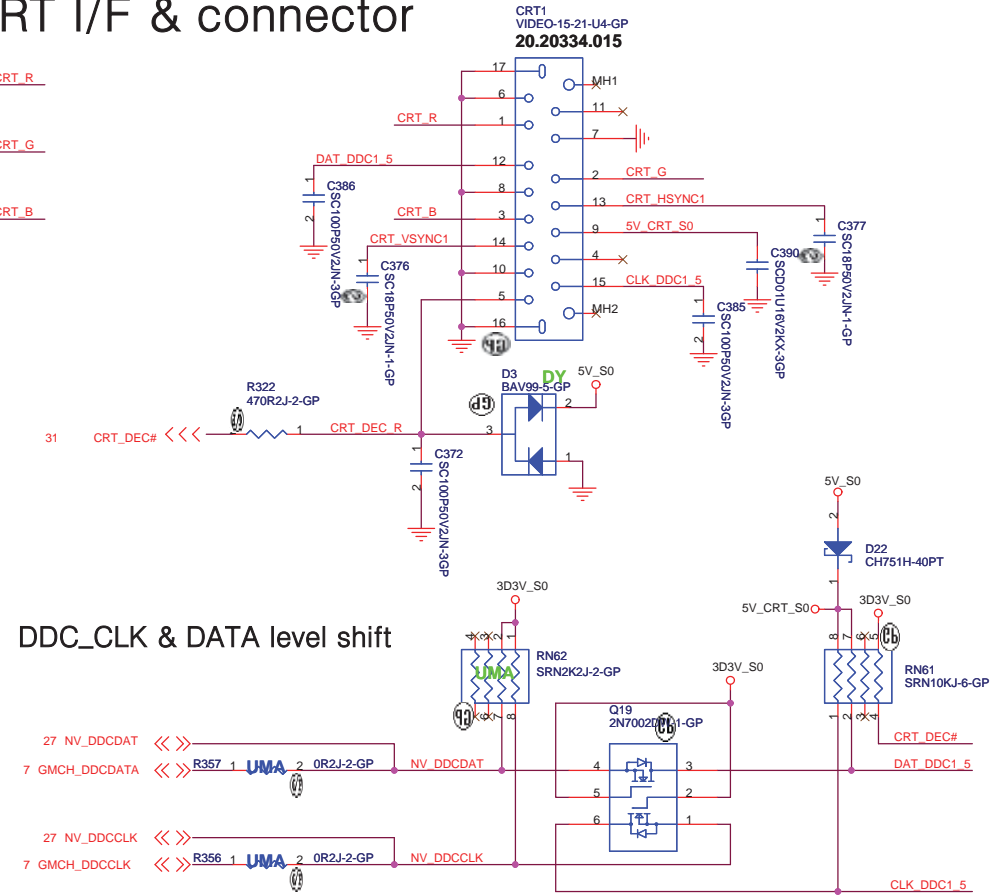
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

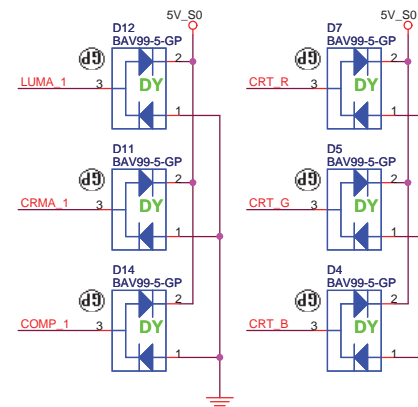
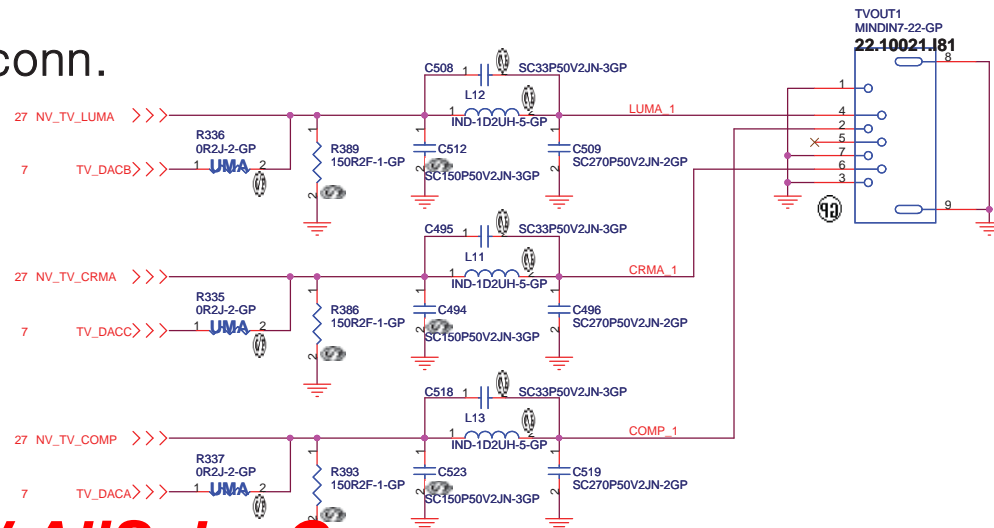
Hsync & Vsync level shift



DDC_CLK & DATA level shift




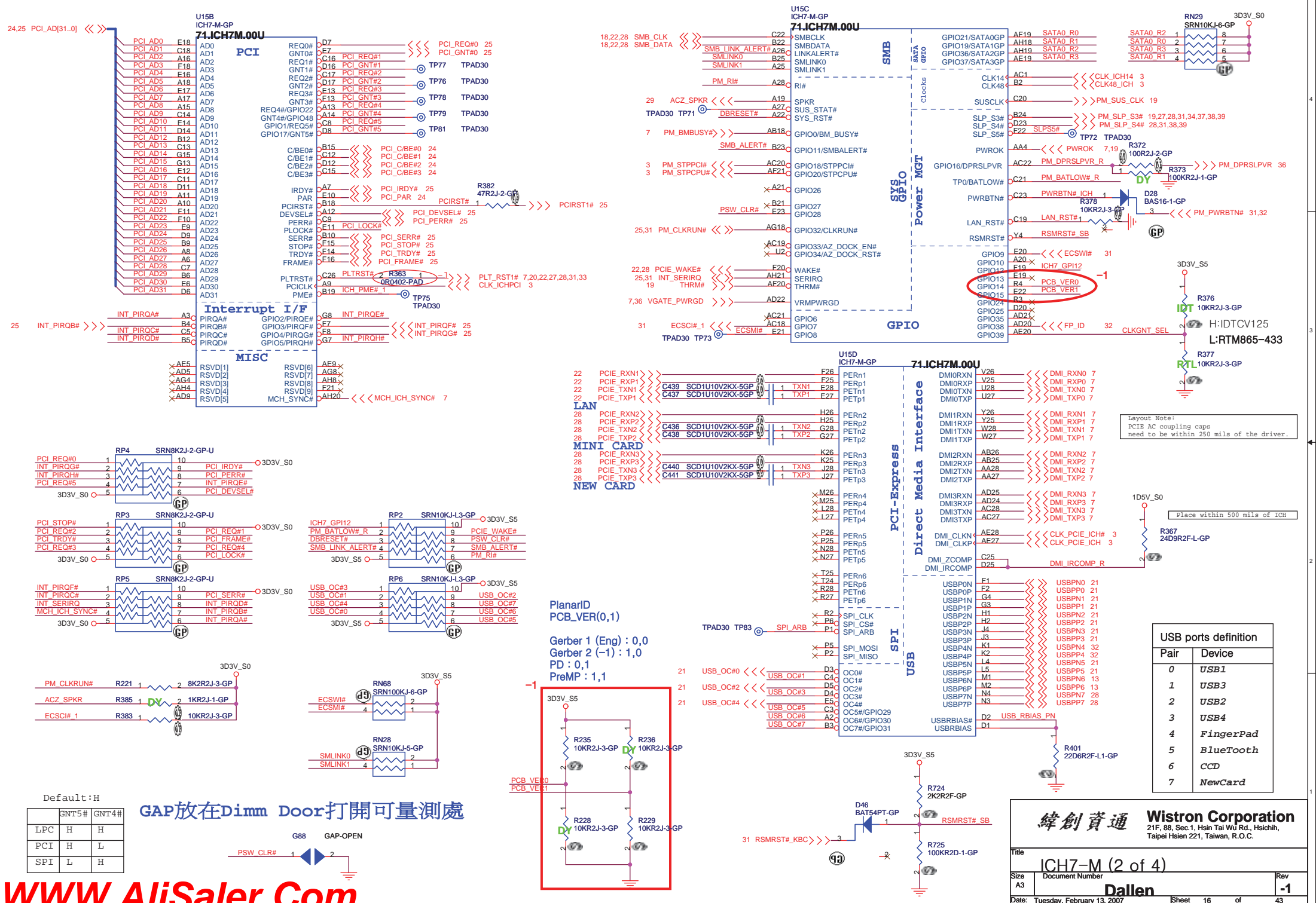
TV conn.



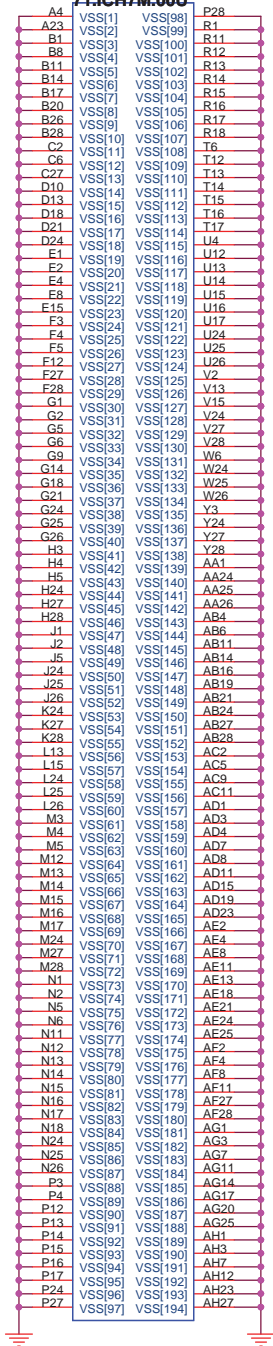
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CRT/TV Connector		
Size A3	Document Number Dallen	Rev -1
Date: Tuesday, February 13, 2007	Sheet 14	of 43

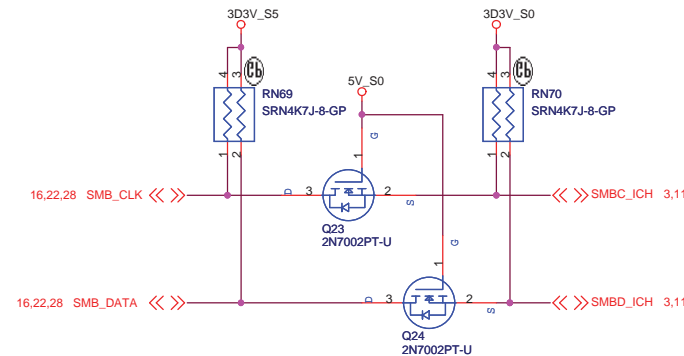
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Title			
ICH7-M (1 of 4)			
Size A3	Document Number		Rev
	Dallen		-1
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U15E
ICH7-M-GP
Z1.ICH7M.00U



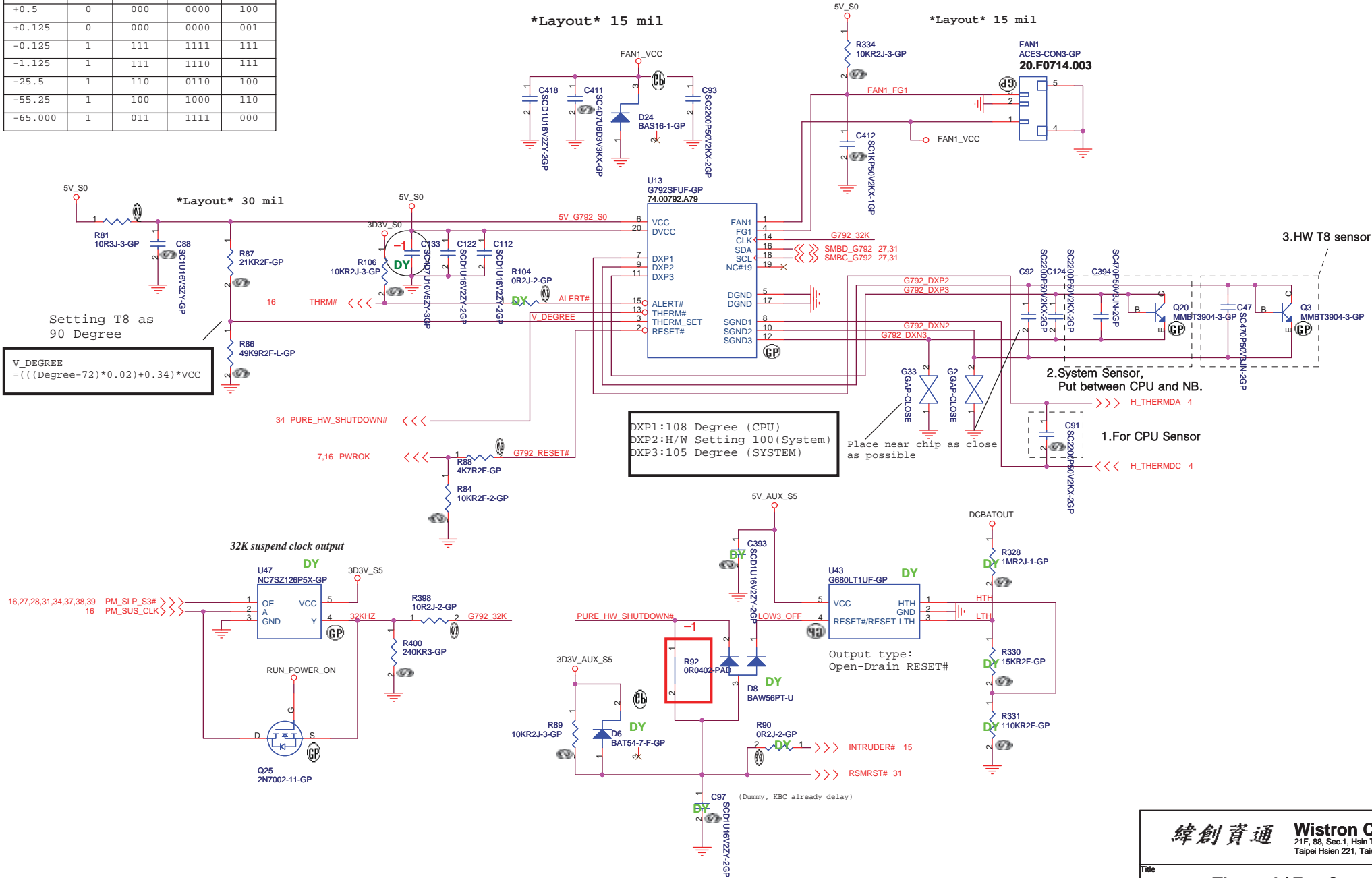
SMBUS



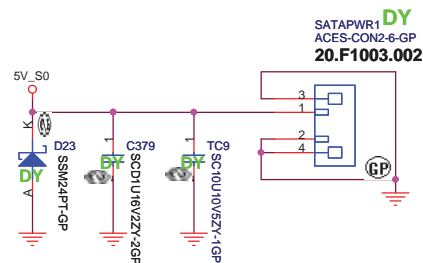
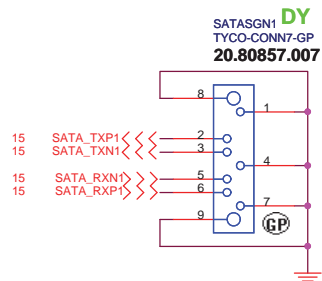
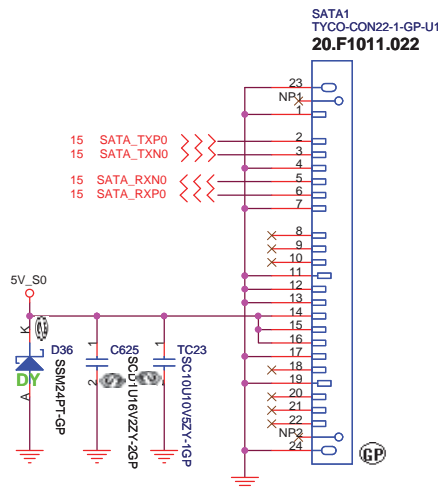
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ICH7-M (4 of 4)	
Size	Document Number	Dallen		Rev
A3				-1
Date: Tuesday, February 13, 2007		Sheet	18	of 43

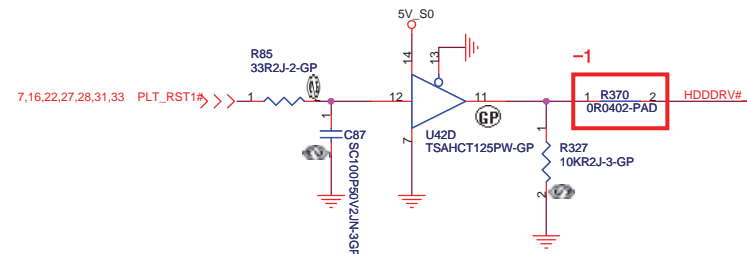
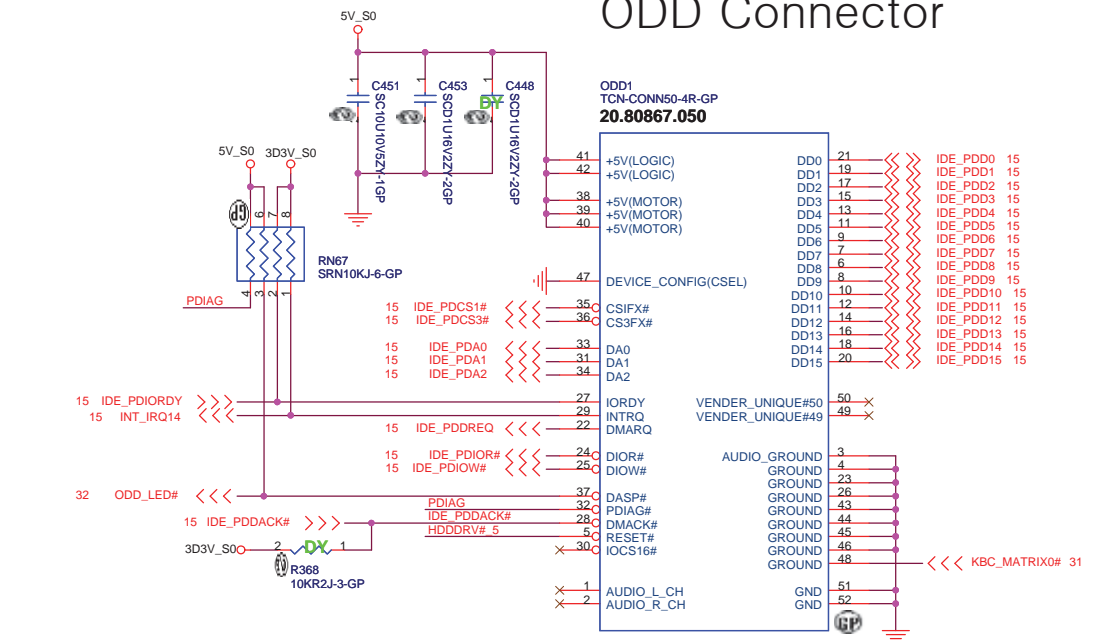
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



SATA HD Connector

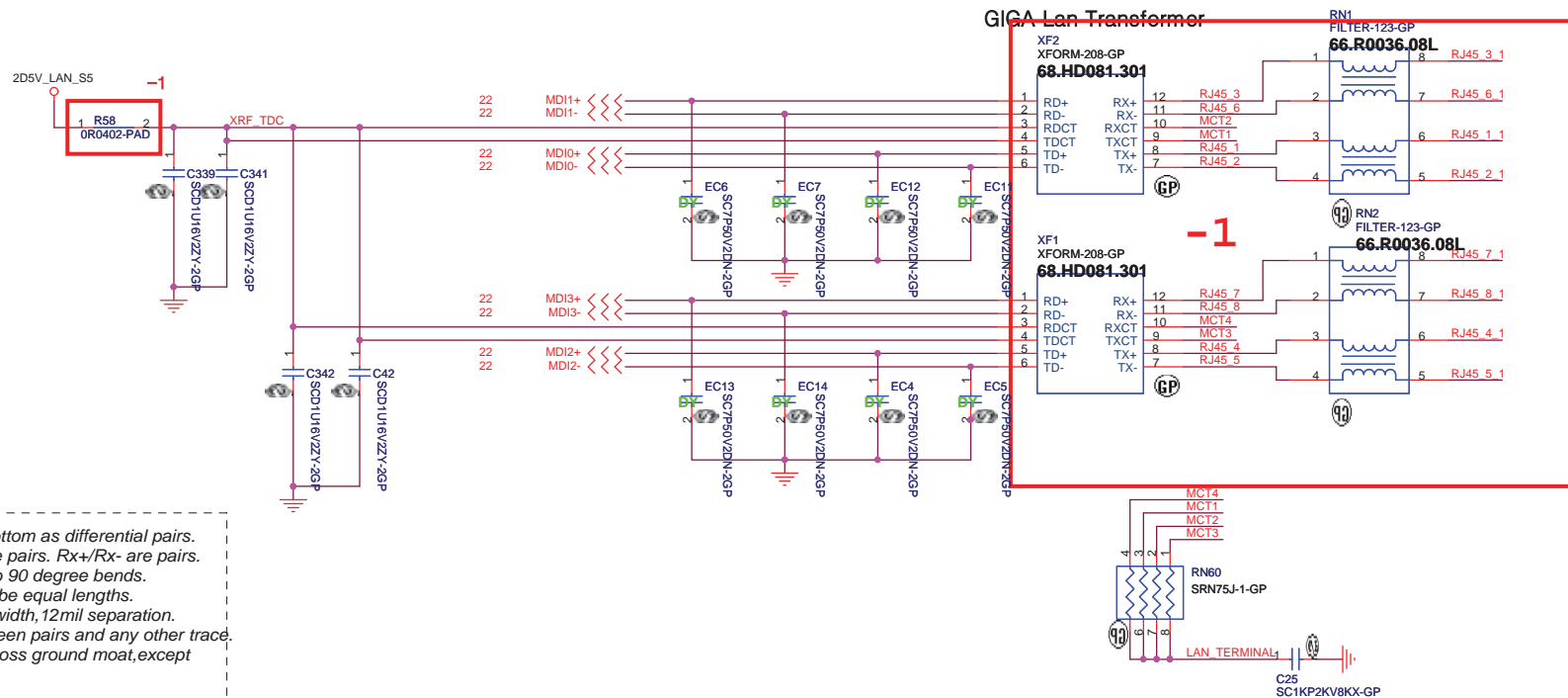
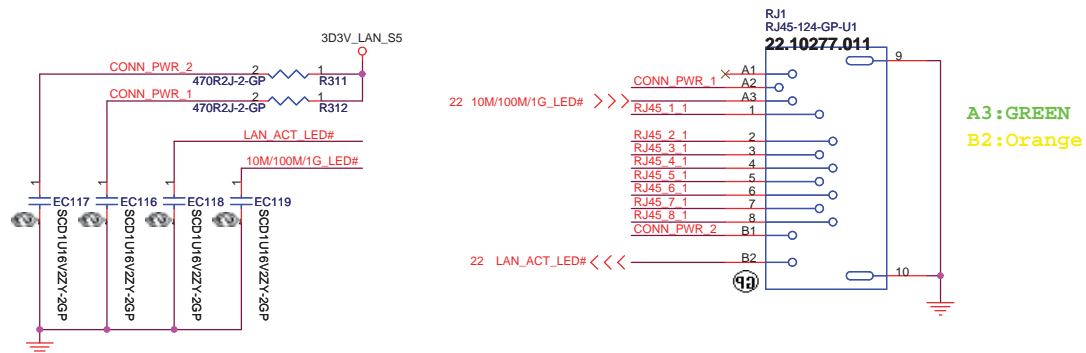


ODD Connector



LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

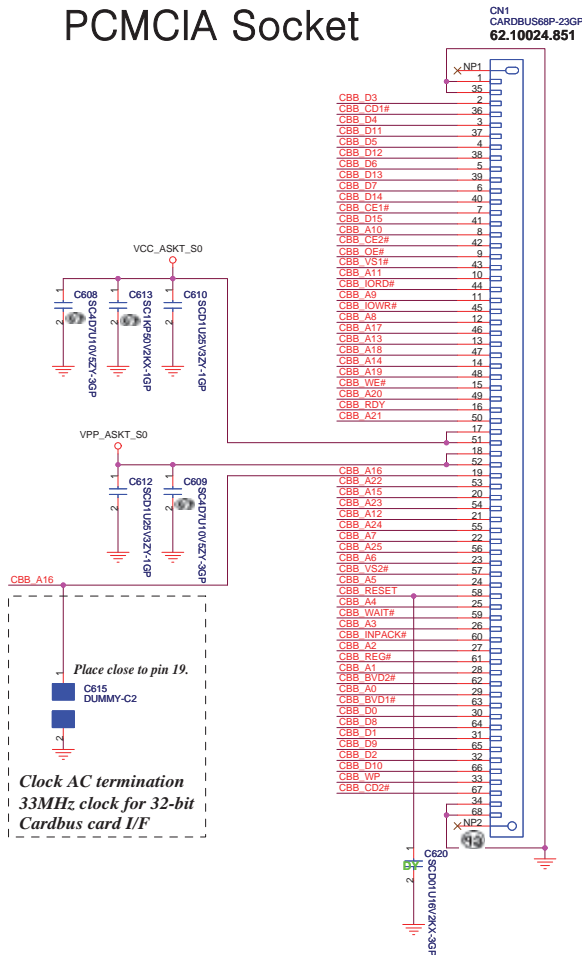
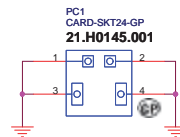
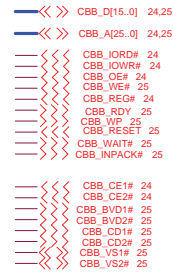
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

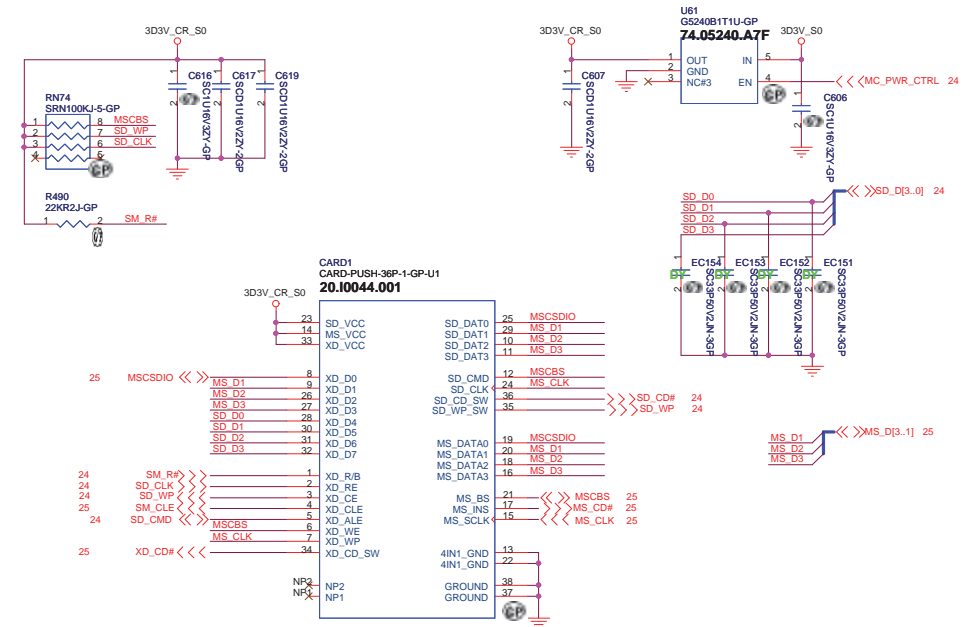
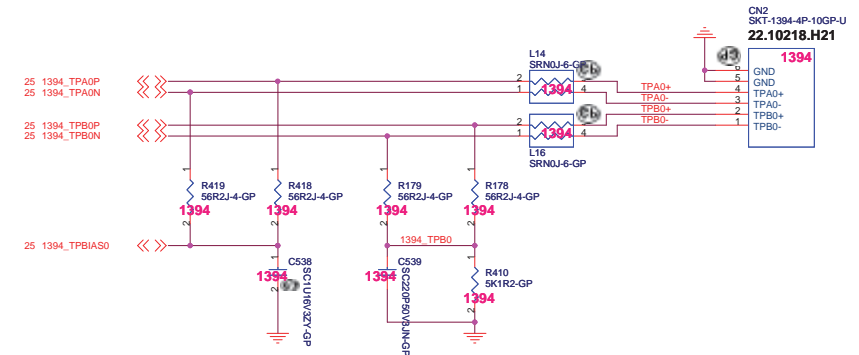
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

PCMCIA Socket

**Cardbus I/F**

1394 Connector



XD
MS / MS PRO
SD / SD IO / MMC

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCMCIA / 1394 / CARD READER			
Size	Document Number	Rev	
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Date:	Tuesday, February 13, 2007	Sheet	26 of 43

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

13 LCD_TXBOUT0+
13 LCD_TXBOUT0-
13 LCD_TXBOUT1+
13 LCD_TXBOUT1-
13 LCD_TXBOUT2+
13 LCD_TXBOUT2-

13 LCD_TXBCLK+
13 LCD_TXBCLK-
14 NV_BLUE
14 NV_GREEN
14 NV_RED

14 NV_TV_COMP
14 NV_TV_LUMA
14 NV_TV_CRMA

LCD_TXACKL- 13
LCD_TXACKL+ 13
LCD_TXAOUT2- 13
LCD_TXAOUT2+ 13
LCD_TXAOUT1- 13
LCD_TXAOUT1+ 13
LCD_TXAOUT0- 13
LCD_TXAOUT0+ 13

>>> NV_EDID_DAT 13

>>> NV_EDID_CLK 13

>>> NV_LCDVDD_ON 13

>>> NV_BLOK 31

>>> NV_DVI_DAT 42

>>> NV_DVI_CLK 42

>>> NV_DVI_CLK 42

>>> NV_DVI_CLK 42

>>> NV_DVI_CLK 42

>>> NV_DVI_CLK 42

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>>> NV_DVI_CLK 42

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>>> NV_DVI_CLK 42

>>> NV_DVI_CLK 42

>>> NV_DVI_CLK 42

EMI REQUEST

TMDS A_TX0+ 1 4
TMDS A_TX0- 1 2
SRN33J-5-GP-U 3
TMDS A_TX1+ 1 1
TMDS A_TX1- 1 2
SRN33J-5-GP-U 3
TMDS A_TX2+ 1 1
TMDS A_TX2- 1 2
SRN33J-5-GP-U 3
TMDS A_TXC+ 1 1
TMDS A_TXC- 1 2
SRN33J-5-GP-U 3

ERN* 要靠近MXM conn.

<<< DVI_A_HPD 42

TMDS B_TX0+ TP69 TPAD30

TMDS B_TX0- TP68 TPAD30

TMDS B_TX1+ TP65 TPAD30

TMDS B_TX1- TP54 TPAD30

TMDS B_TX2+ TP62 TPAD30

TMDS B_TX2- TP61 TPAD30

TMDS B_TXC+ TP58 TPAD30

TMDS B_TXC- TP52 TPAD30

DVI B_HPD TP64 TPAD30

TMDS B_TXC+ TP53 TPAD30

TMDS B_TXC- TP52 TPAD30

TMDS B_TXC+ TP53 TPAD30

TMDS B_TXC- TP52 TPAD30

TMDS B_TXC+ TP53 TPAD30

TMDS B_TXC- TP52 TPAD30

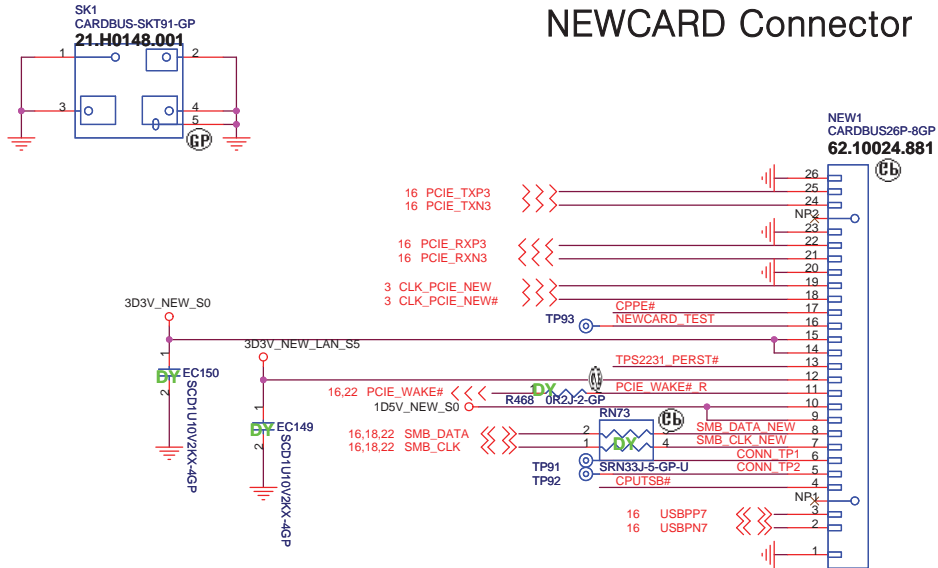
TMDS B_TXC+ TP53 TPAD30

TMDS B_TXC- TP52 TPAD30

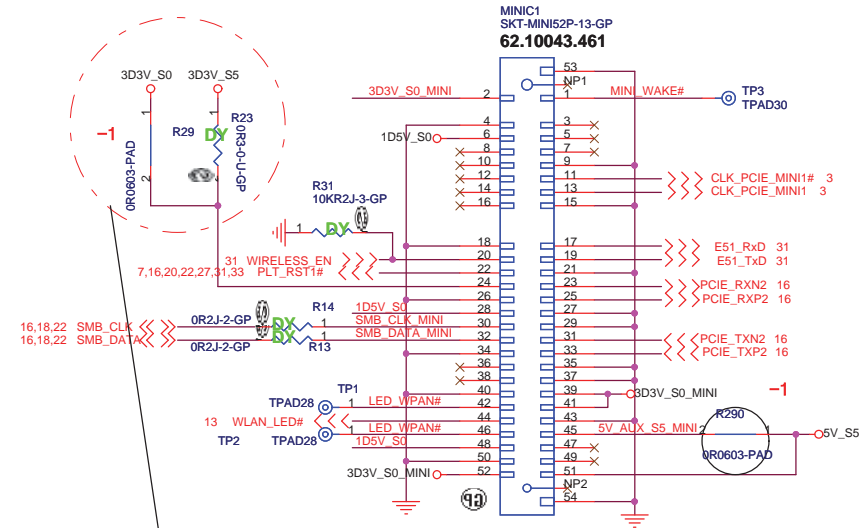
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Title		
Graphic MXM CONN		
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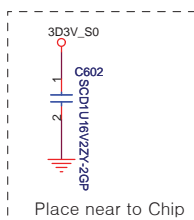
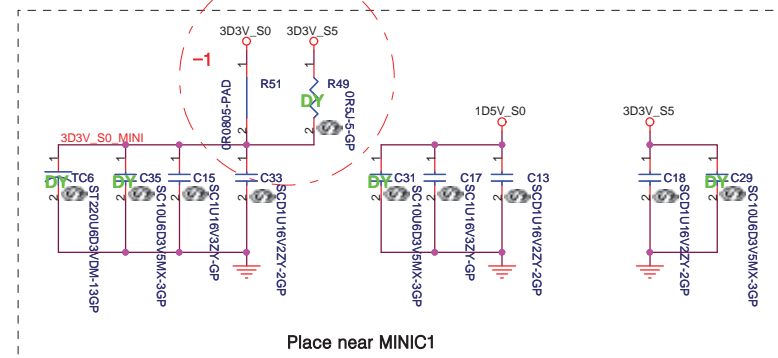
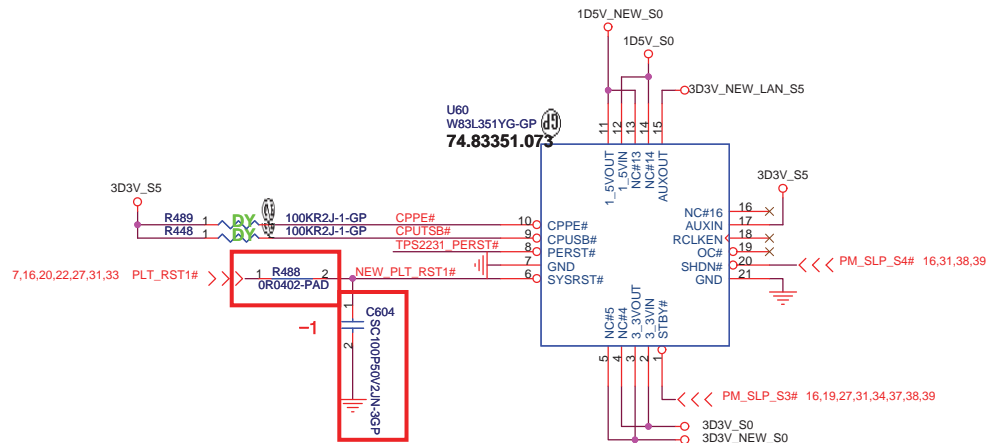
NEWCARD Connector



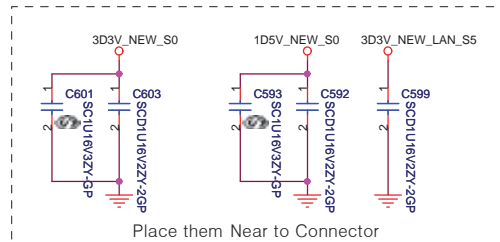
Mini Card Connector



PCIE Mini Card For WLAN w/o iAMT, TV or 3G



Place near to Chip



Place them Near to Connector

Audio OP Amplifier

R,L 1.5W Speaker

mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

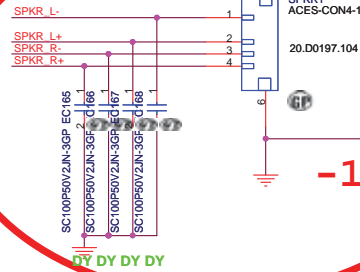
R,L 1W Speaker

mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

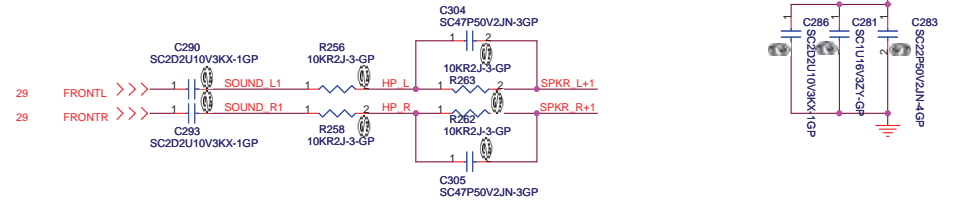
R,L 1.2W Speaker

mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

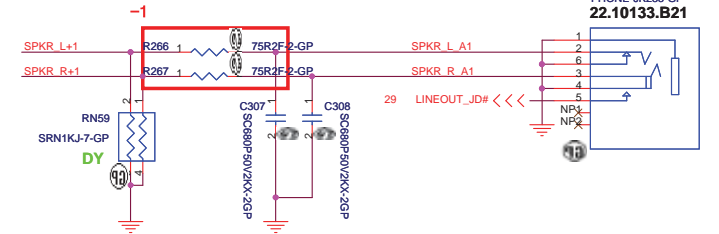
Internal Speaker



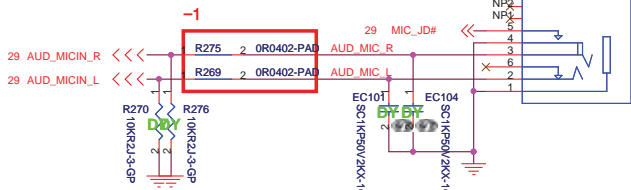
KBC_MUTE_GPIO8



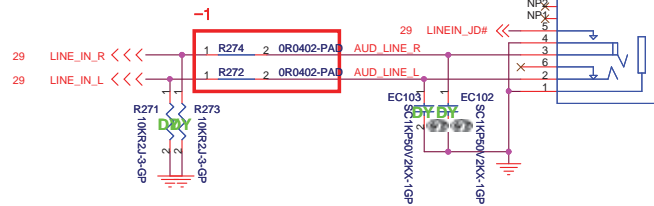
LINE OUT



MIC IN

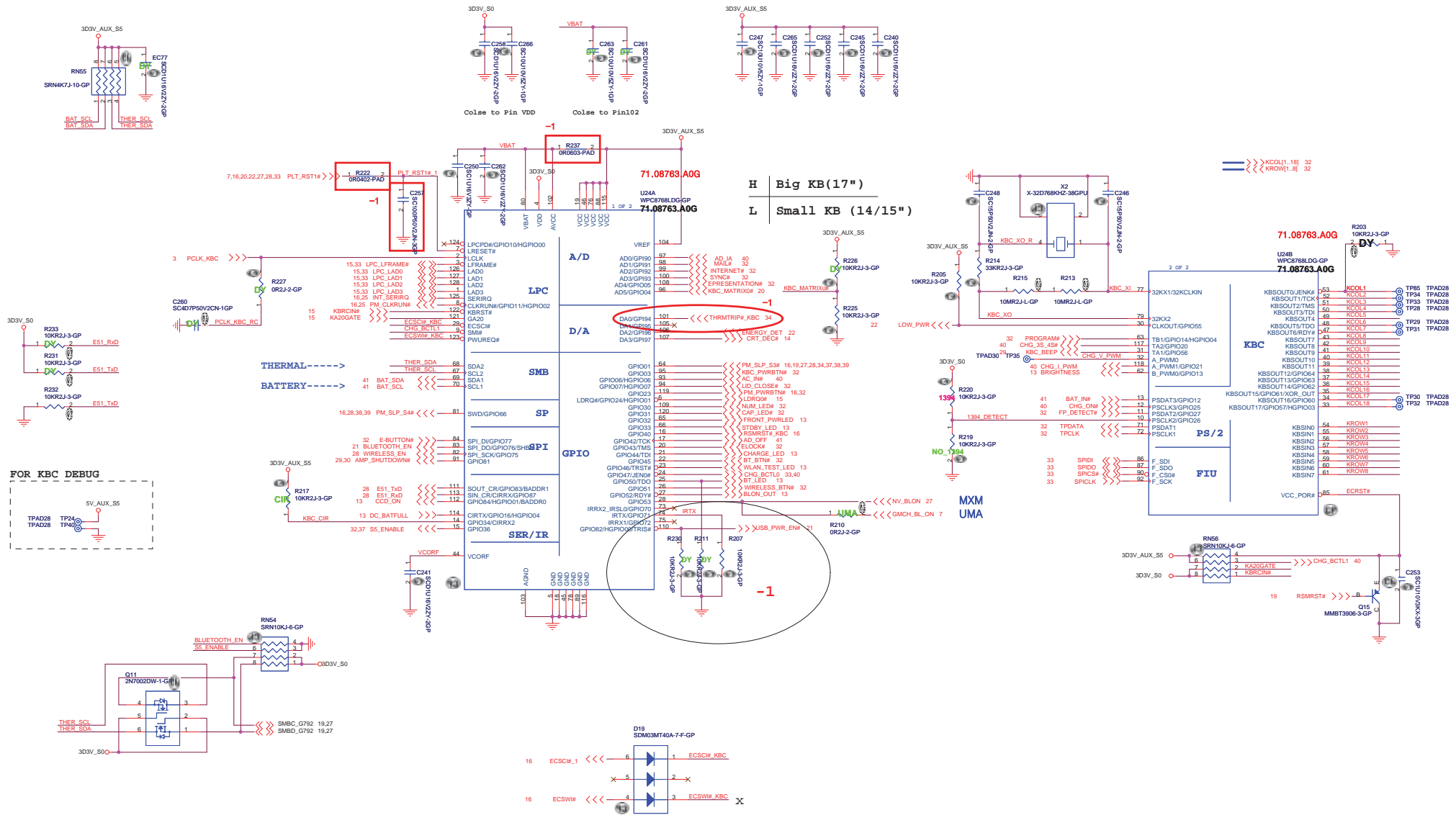


LINE IN



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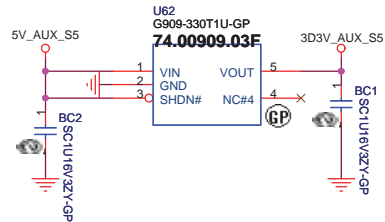
Title	AUDIO AMP AND JACK		
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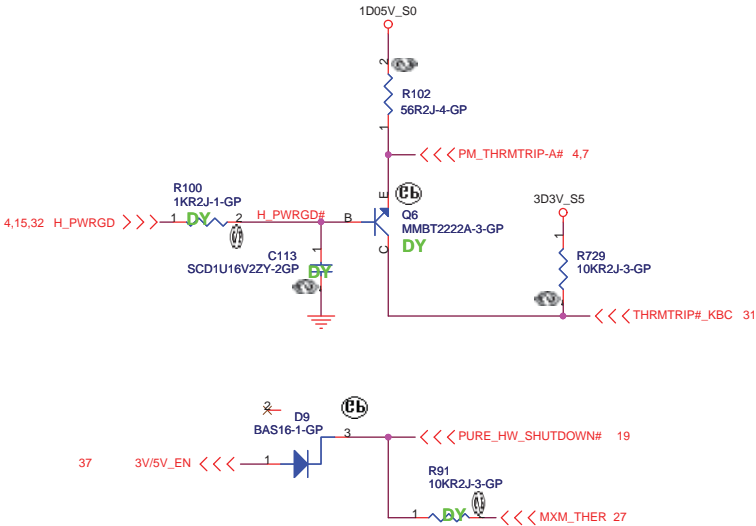
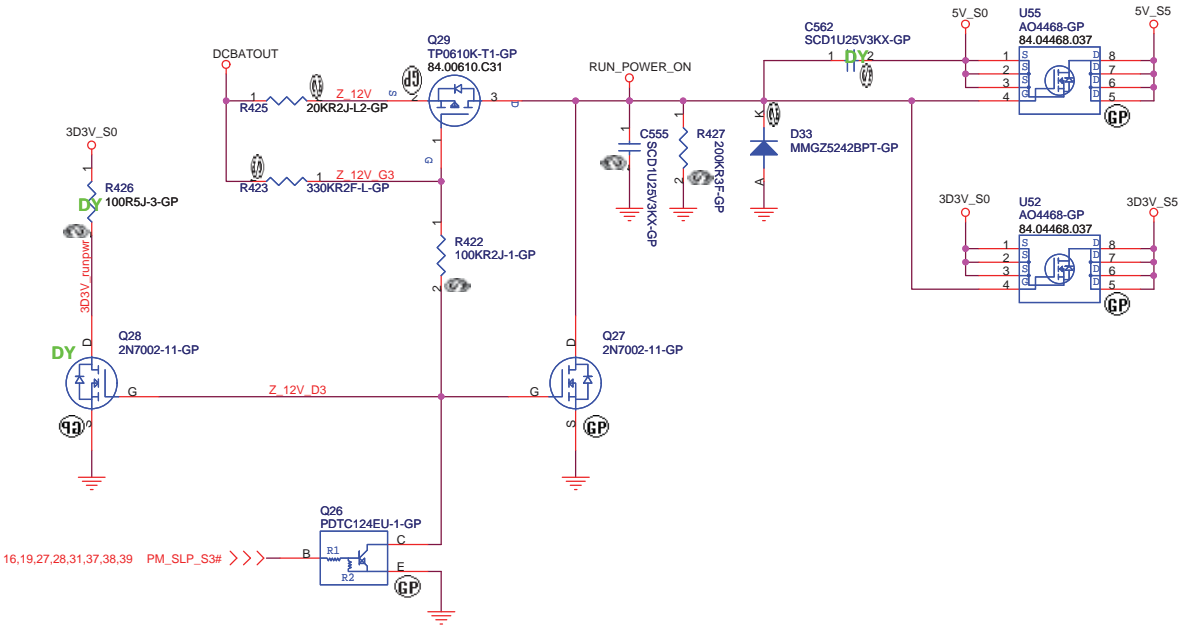
Aux Power

3D3V_AUX_S5

I max = 150 mA



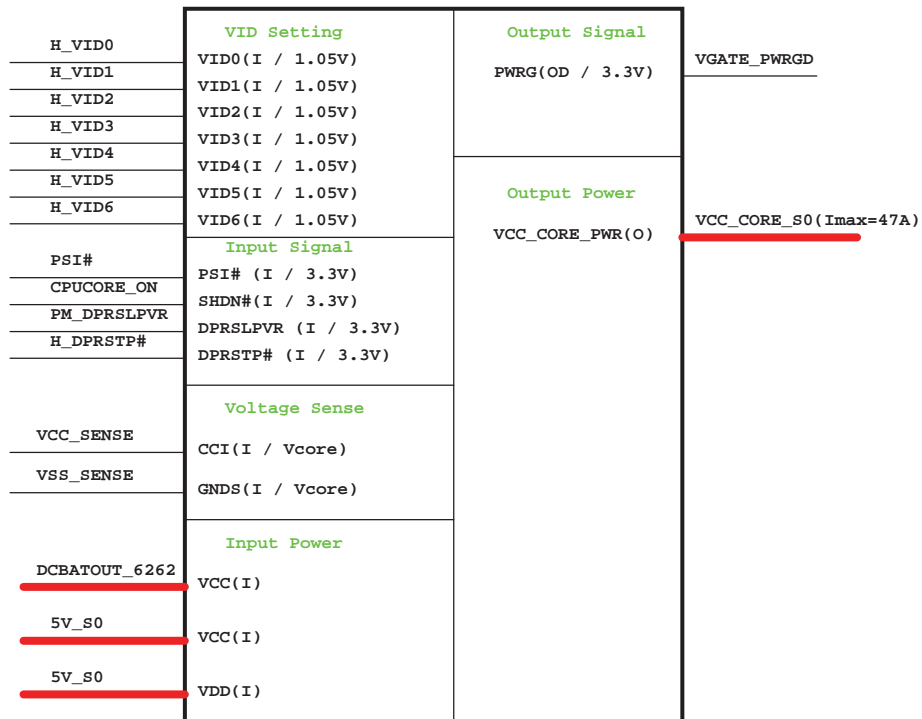
Run Power



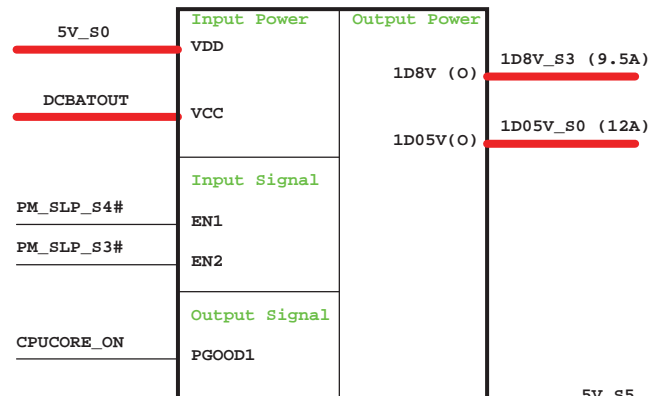
5V_S0

3D3V_S0

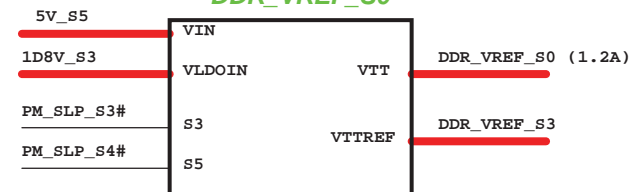
CPU_CORE
MAX8770



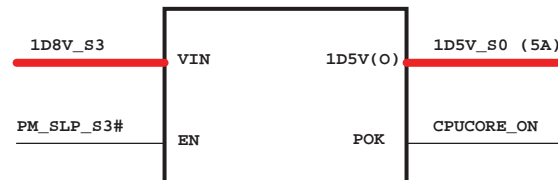
MAX8717
1D8V_S3 / 1D05V_S0



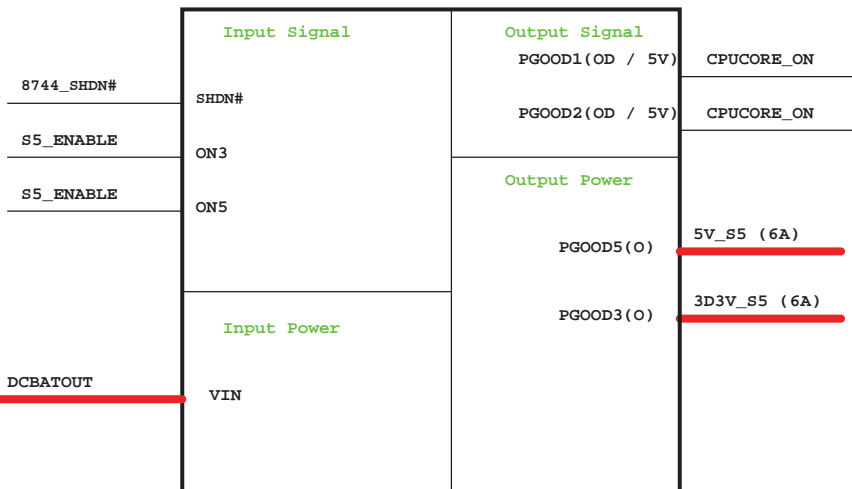
TPS51100
DDR_VREF_S0



APL5912
1D5V_S0



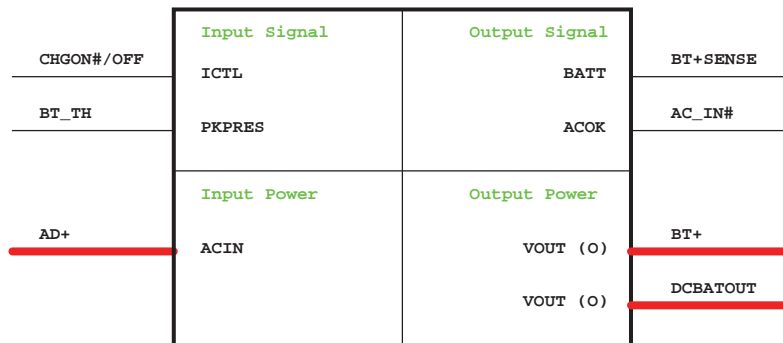
MAX8744
5V_S5 / 3D3V_S5

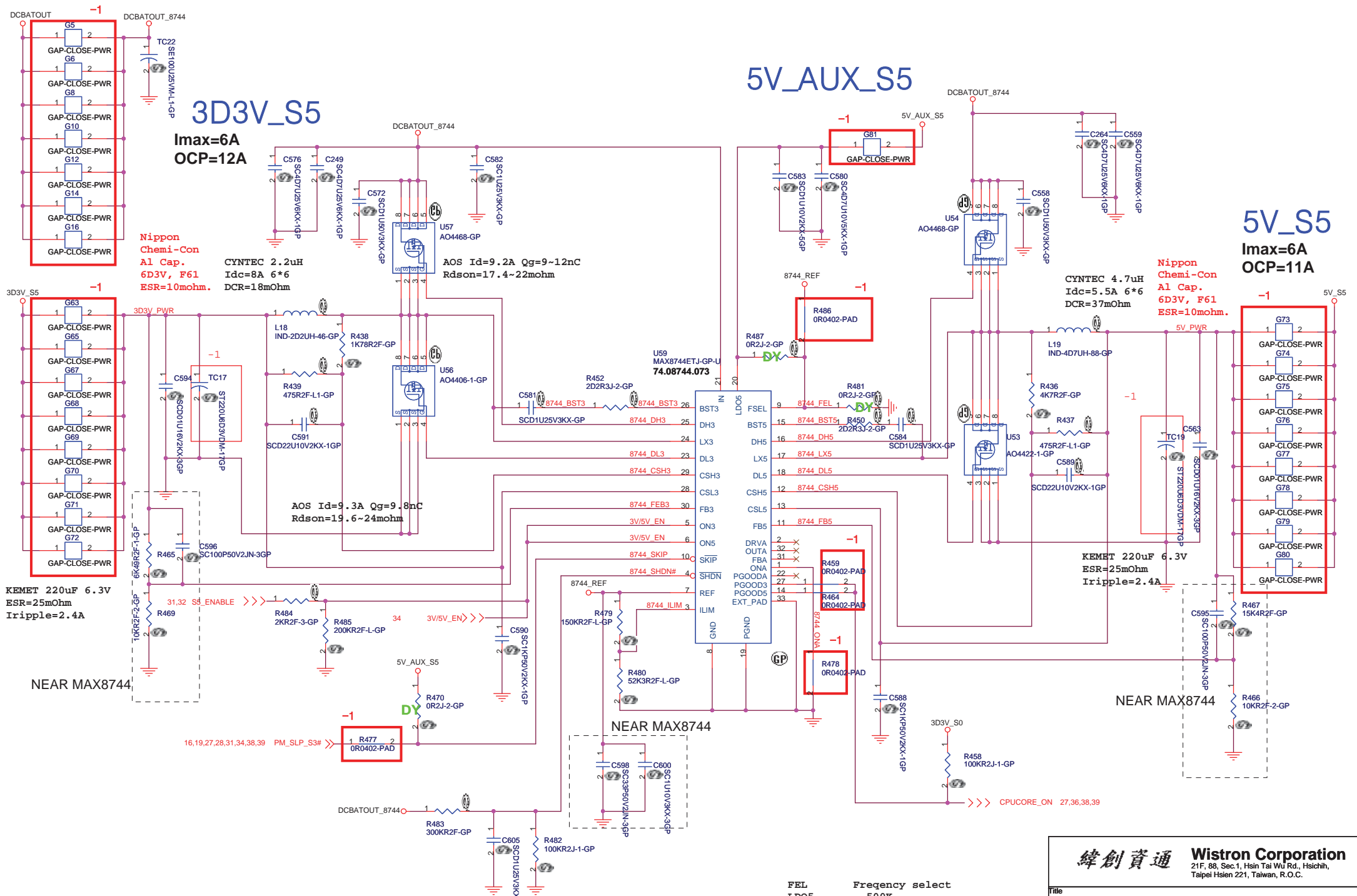


APL5312
2D5V_S0



Charger ISL6255

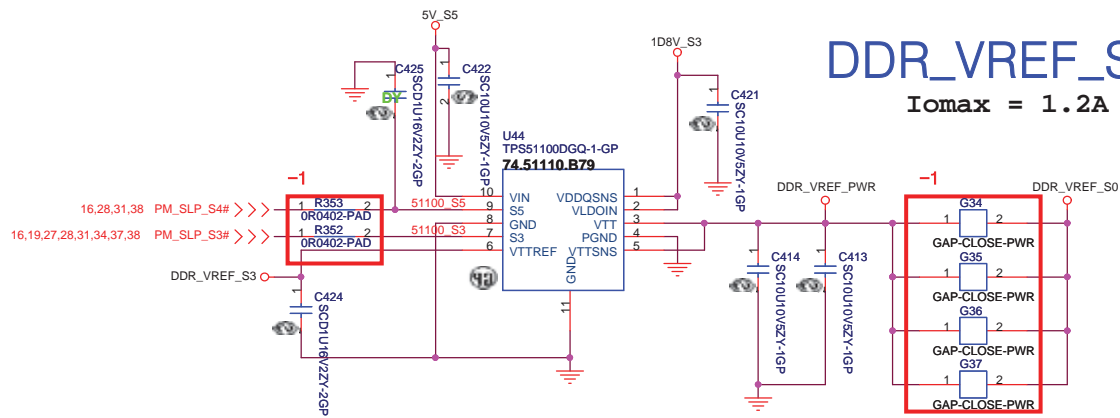




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DDR_VREF_S0

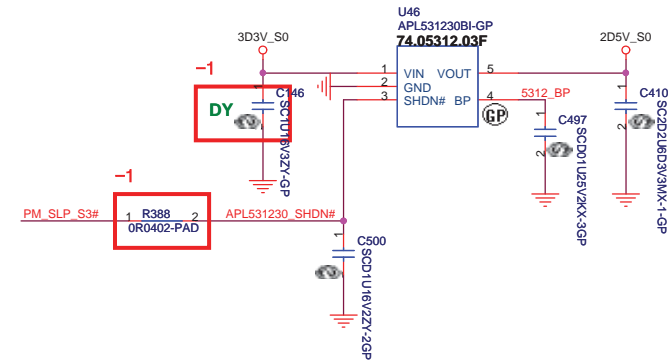
I_{omax} = 1.2A



DDR_VREF_S3

2D5V_S0

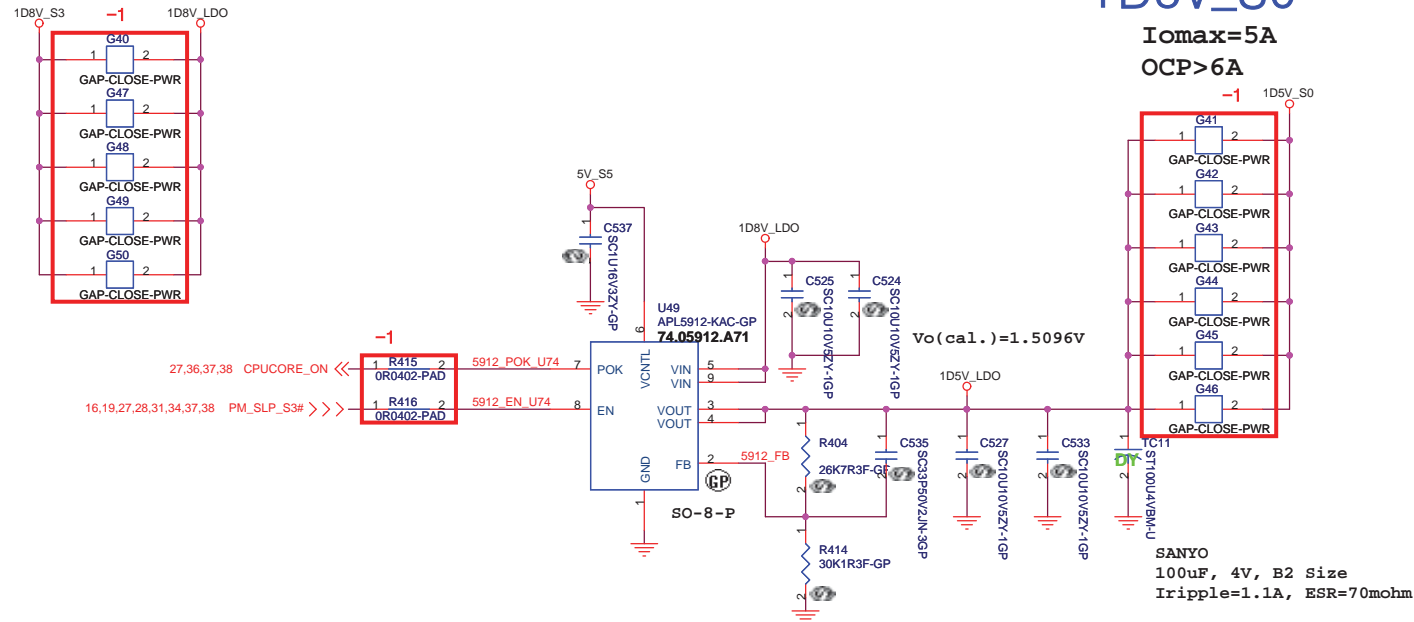
I_{omax} = 130mA



1D5V_S0

I_{omax}=5A

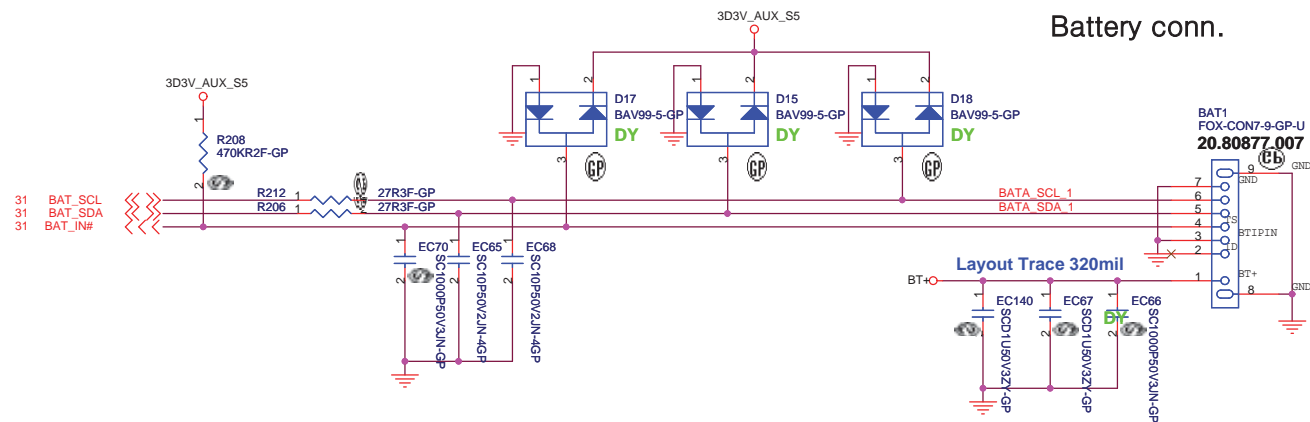
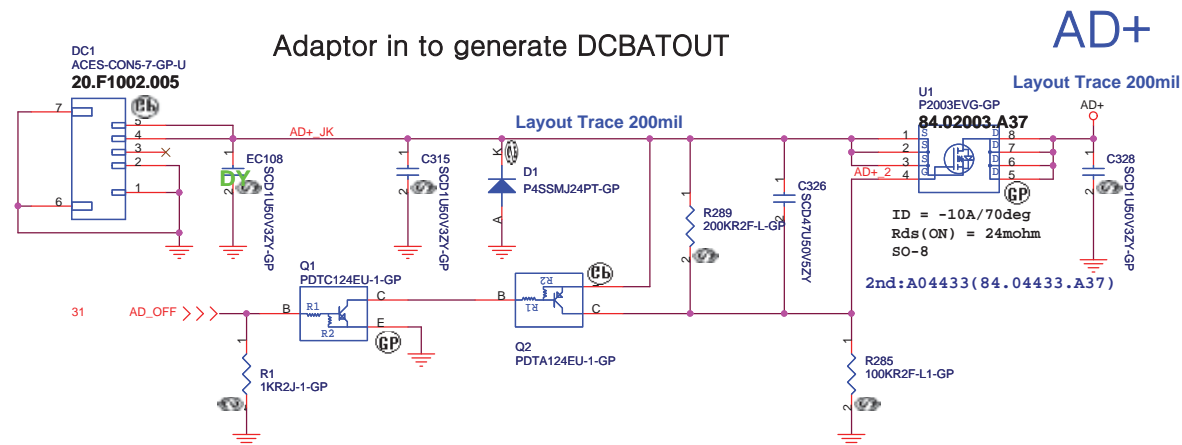
OCP>6A

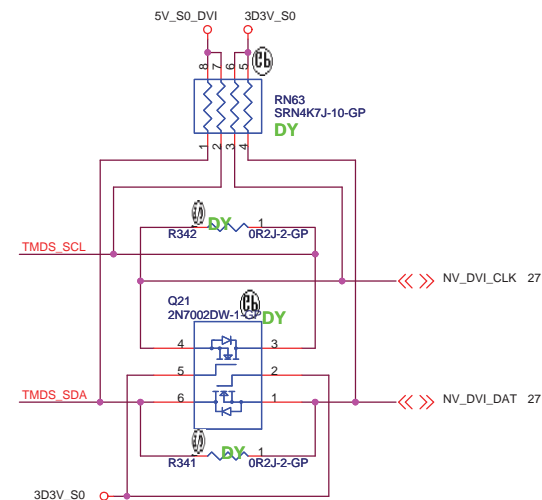
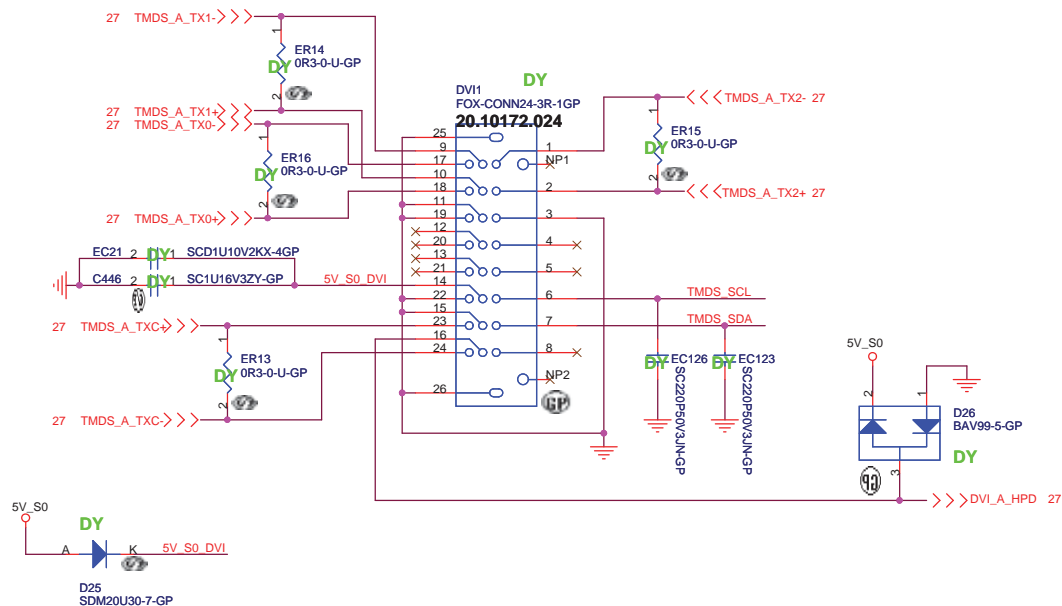


$$V_o = 0.8 * (1 + (R1/R2))$$

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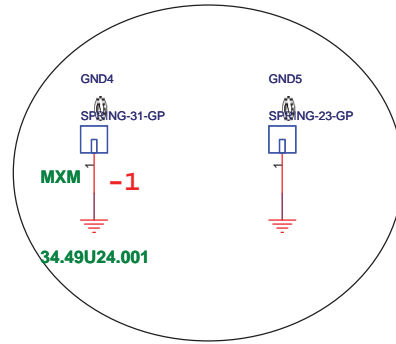
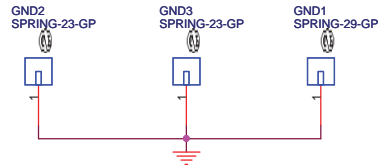
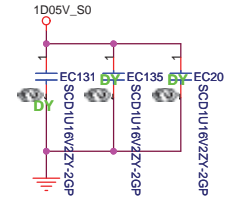
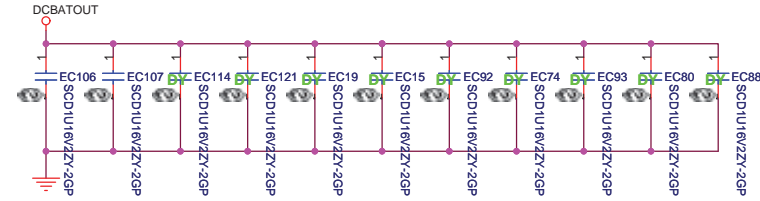
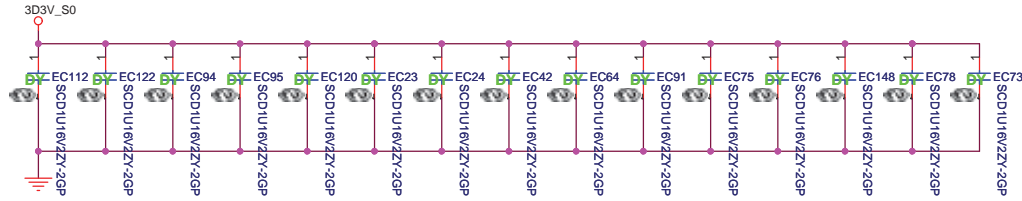
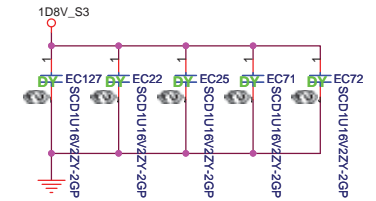
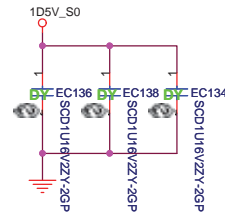
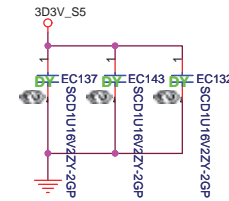
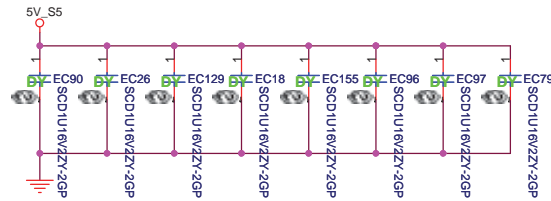
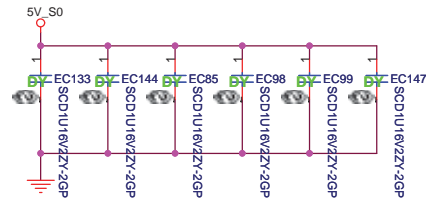
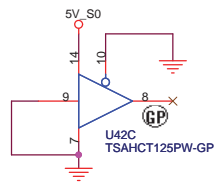
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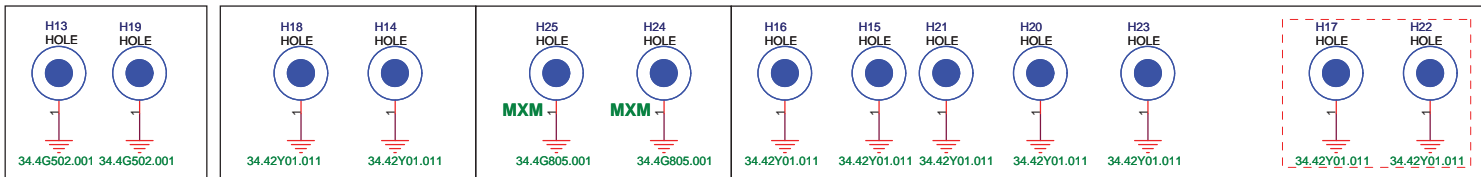
Title			DVI connector	
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Spring

GND 1 : 34.42T14.001
GND 2/3 : 34.39S07.003

MINI CARD



Fan

